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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,814	12/11/2003	Nobuaki Tokushige	900-489	5881
23117	7590	09/19/2005		
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			EXAMINER DANG, TRUNG Q	
			ART UNIT 2823	PAPER NUMBER
DATE MAILED: 09/19/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/732,814

Applicant(s)

TOKUSHIGE, NOBUAKI

Examiner

Trung Dang

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/23/05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4 and 6 is/are rejected.
- 7) ☒ Claim(s) 2,5 and 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueda et al (US 2002/0031897 cited by applicant).

With reference to Figs. 1C-1D, the reference teaches a semiconductor device comprising:

a semiconductor substrate 1 providing a semiconductor element, and the semiconductor substrate having a thickness that allows the substrate to secure flexibility and/or to have light transparency; and
a hard film 3 which covers a part or the entirety of a peripheral side of the semiconductor substrate and which has top and bottom surfaces in approximately the same planes as those of the top and bottom surfaces of the semiconductor substrate (Fig. 1C),
wherein the entire peripheral side of the semiconductor substrate covered with the hard film is processed so as to be perpendicular or substantially perpendicular to the surface of the semiconductor substrate (Fig. 1D).

Note that the semiconductor substrate 1 has a thickness of about 15 μm (para. [0018]) that is within the thickness range disclosed in the instant specification, hence the semiconductor substrate 1 would inherently allows the substrate to secure flexibility/and or to have light transparency as claimed. Furthermore, it is known in the art of manufacturing semiconductor device, semiconductor wafer is fabricated into a plurality of discrete die separated each other by scribe lines (Dando's reference of record is cited herein, merely for the purpose of showing this fact) therefore when the semiconductor substrate 1 is divided into individual chip by dicing, the cutting must be performed along entire peripheral side of the semiconductor substrate.

For claim 4, with respect to the claimed limitation regarding the hard film is a silicon oxide film, see paragraph [0017].

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Qi et al. (US 6,649,445).

With reference to Figs. 3-11, the reference anticipates the claim in that it discloses a manufacturing method for a semiconductor device, comprising the steps of:

(a) forming a recess in a semiconductor substrate, the semiconductor substrate having a semiconductor element, the recess being located in a region of the semiconductor substrate where the semiconductor element is not formed, the recess having side walls that are perpendicular to a surface of the semiconductor substrate (Fig. 3);

- (b) filling the recess with a material of a hard film 40 (Fig. 4 and col. 3, line 28);
- (c) adhering a support substrate 82 to the surface of the semiconductor substrate having the recess defined therein, and making the bottom surface of the semiconductor substrate retrogress until a bottom surface of the hard film is exposed (Figs. 8-9);
- (d) after making the bottom surface of the semiconductor substrate retrogress until the bottom surface of the hard film is exposed, removing the support substrate from the semiconductor substrate (Fig. 9); and
- (e) after removing the support substrate, dividing the semiconductor substrate into pieces by cutting the hard film (Fig. 10).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. as above in view of Jenq (US 6,204,146).

This rejection is made with respect to the claimed limitation regarding the hard film is a silicon nitride film.

Ueda teaches a semiconductor device as described above. Ueda differs from the claim in the material of the hard film 3 is of silicon oxide rather than silicon nitride as claimed.

Jenq teaches isolation trench is filled with silicon nitride 208 and silicon oxide 210a (Fig. 2C and col. 3, lines 3-21). The inclusion of silicon nitride layer 208 in an oxide-filled isolation trench has advantages such as the nitride layer acts as an oxygen barrier to prevent non-bonded oxygen molecule from penetrating into the active region, hence the conductivity of the device would not be effected (col. 3, lines 39-42).

It would have been obvious to one of ordinary skill in the art to modify Ueda's teaching by including a silicon nitride layer in the oxide-filled isolation trench 3 as suggested by Jenq because of the benefit mentioned above.

Allowable Subject Matter

6. Claims 2, 5, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2, 5 and 7 are allowable over prior art of record because the prior art fail to teach or suggest the claimed subject matter which includes the claimed feature

regarding a through hole formed in the hard film and a through electrode formed in the through hole.

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 6 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Trung Dang
Primary Examiner
Art Unit 2823

09/17/05